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| 09/917,661 | 07/31/2001 | Praveen K. Parvathala | 219.39515X00 | 1090 |

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| EXAMINER | |
|---|---|
| TABONE JR, JOHN J | |
| **ART UNIT** | **PAPER NUMBER** |
| 2133 | |

DATE MAILED: 12/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/917,661 | PARVATHALA ET AL. | |
| | Examiner | Art Unit | |
| | John J. Tabone, Jr. | 2133 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *18 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. The pending claims 1-38 have been examined.

### *Claim Rejections - 35 USC § 112*

2. The rejections of claims 1, 11, 21 and 31 rejected under 35 USC § 112, second paragraph, per paper 6 ¶ 2 have been overcome by the Applicant by amending these claims to provide clarity and provided a paragraph of explanation from the specification to provide further clarity. The rejections have been withdrawn.

### *Response to Arguments*

3. Applicant's arguments filed 6/18/2004 with respect to claims 1-3, 11-13, 21-23, and 31-33 have been fully considered but they are not persuasive.

Claims 1, 11 and 21:

The Applicant states that the Williams reference does not disclose, teach, or suggest the subject of independent claim 1 as amended, including for example, "executing software within the FRIT kernel on the complex device under test." The Examiner asserts that Williams teaches the limitation cited in amended claims 1, 11 and 21. Given the broadest interpretation of the claim language the Examiner reads that the FRIT kernel is converted to kernel test patterns which is stored in tester memory. The kernel test patterns are then loaded into memory that resides on the complex device under test. The software within the FRIT kernel, which converts the FRIT kernel into

kernel test patterns, executes those kernel test patterns on the complex device under test. Williams teaches these limitations in that Williams teaches the ATPG tool 12 is generally described as a computer system that is programmed to execute ATPG processes (software within the FRIT kernel) whose primary purpose is to efficiently generate test vectors (kernel test patterns). Williams further teaches the ATPG tool 12 writes the test patterns into a first memory (memory1) of tester 14 (tester memory). (Page 3-4, ¶ 33-35). Williams discloses the tester 14 scans test vectors (loading kernel test patterns) into memory cells of the DUT 16 (on-board memory) during test mode and the DUT 16 is then operated (executing functional test) which generates a set of outputs. The Examiner contends that software within the FRIT kernel is executed by the ATPG tool 12 to convert the FRIT kernel into kernel test patterns which is stored in tester memory. There are no other limitations in these claims which would lead the Examiner to a different interpretation. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). It is the Examiner's conclusion that claims 1, 11 and 21 as amended are not patentably distinct or non-obvious over the prior art of record in view of Williams et al. (US-2002/0093356). Therefore, the rejection is maintained.

Claim 31:

The Applicant states that the Williams reference does not disclose, teach, or suggest the subject of independent claim 31 as amended, including for example, "a processor to perform a ... test of the complex device under test (DUT) upon execution

of the FRIT kernel." The Examiner asserts that Williams teaches the limitation cited in amended claim 31 as stated in the response to claims 1, 11 and 21 above. Furthermore, Williams teaches the ATPG tool 12 is generally described as a computer system (a processor) that is programmed to execute ATPG processes (software within the FRIT kernel) whose primary purpose is to efficiently generate test vectors (kernel test patterns). The Examiner contends that software within the FRIT kernel is executed by the ATPG tool 12, which includes a processor, to convert the FRIT kernel into kernel test patterns which is stored in tester memory. There are no other limitations in these claims which would lead the Examiner to a different interpretation. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). It is the Examiner's conclusion that claim 31 as amended is not patentably distinct or non-obvious over the prior art of record in view of Williams et al. (US-2002/0093356). Therefore, the rejection is maintained.

Claims 2, 3, 12, 13, 22, 23, 32 and 33:

Regarding these claims, the Applicant states the office action incorrectly equates the ATPG tool 12 of Williams with the FRIT kernel/SBE of the claimed invention. The Applicant further states the ATPG tool of Williams is external to the device under test, whereas the FRIT kernel/SBE of the claimed invention is resident within the device under test when the test is run. The Examiner asserts that Williams teaches the limitation cited in claims 2, 3, 12, 13, 22, 23, 32 and 33 as stated in the response to claims 1, 11 and 21 above. There are no claim language within these claim limitations to

lead the Examiner to interpret the FRIT kernel/SBE of the claimed invention is resident within the device under test when the test is run. The Applicant is reminded that although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). It is the Examiner's conclusion that claims 2, 3, 12, 13, 22, 23, 32 and 33 are not patentably distinct or non-obvious over the prior art of record in view of Williams et al. (US-2002/0093356). Therefore, the rejection is maintained.

***Claim Rejections - 35 USC § 102***

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-3, 6, 11-13, 16, 21-23, 26, and 31-33 are rejected under 35 U.S.C. 102(e) as being anticipated by Williams et al. (US-2002/0093356).

Claims 1, 11, 21 and 31:

Williams teaches the ATPG tool 12 is generally described as a computer system that is programmed to execute ATPG processes (FRIT kernel) whose primary purpose is to efficiently generate test vectors (kernel test patterns). Williams further teaches the ATPG tool 12 writes the test patterns into a first memory (memory1) of tester 14 (tester memory). (Page 3-4, ¶ 33-35). Williams discloses the tester 14 scans test vectors (loading kernel test patterns) into memory cells of the DUT 16 (on-board memory) during test mode and the DUT 16 is then operated (executing functional test) which

generates a set of outputs. Williams further discloses that the tester 14 applies the test patterns to the DUT 16 and examines the real output of the DUT 16 against the expected output (comparing test results with an expected test result). The tester 16 then recalls the output from the DUT 16. The test vectors provide the necessary inputs in order to detect the presence of faults within the DUT 16 (check for manufacturing faults). (Page 4, ¶ 34).

Claims 2, 12, 22, 32 and 33:

Williams teaches the ATPG tool 12 (FRIT kernel/SBE) contains a netlist description 18 of the electronic design that is found within the DUT 16 and can be written in HDL (high level design language) (computer model). Williams further teaches the ATPG tool 12 not only generates test patterns, but during simulation it also captures the expected outputs of the netlist 18 (expected test result obtained from computer modeling) based on the application of these test patterns. (Page 3-4, ¶ 33).

Claims 3, 13 and 23:

These claims have the same limitation as claims 2, 12, 22 above and are rejected per those claims.

Claims 6, 16 and 26:

Williams teaches the DUT 16 is typically an integrated circuit or "chip." A microprocessor is a type of integrated circuit. (Page 3, ¶ 33).

5. Applicant's arguments with respect to claim groups 4, 14, 24 and 34 and 7, 17, 27 and 36 have been considered but are moot in view of the new ground(s) of rejection.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 36 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 36:

This claim recites the limitation "the on-board memory" in line 9. There is insufficient antecedent basis for this limitation in the claim.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 4, 5, 7-10, 14, 15, 17-20, 24, 25, 27-30, 34-37, and 38 rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al. (US-2002/0093356) in view of Gittinger et al. (US-5668815).

Claims 4, 14, 24 and 34:

Williams teaches that program instructions (machine code) executed by the ATPG system can be stored in RAM 102, ROM 103, or the storage device 104. (Page 6, ¶ 52, 53). Williams also teaches the LFSR circuit 230 will generate a reproducible sequence of pseudo random bits and acts like a pre-specified compressed data repository for the random bits of the test pattern (compressed test results). Williams further suggests that testing circuitry, like the LFSR 230, can be incorporated on the DUT 16. (Page 4,5, ¶ 38, 43, 46). Williams does not explicitly teach a test program execution module including test execution directives. However, Williams does teach a central processor 101 (test program execution module) coupled with bus 100 for processing information and instructions. (Page 6, ¶ 52, 53). Gittinger teaches a microcontroller 10 which a processor core 16, a DMA (Direct Memory Access) control unit 20 and an internal memory 30. Gittinger also teaches the DMA control unit 20 (a test program execution module including test execution directives) is employed to initialize internal memory 30 to a selected background pattern and then to perform read and write tests of the background pattern and the complement of the background pattern upon internal memory 30. (Col. 8, lines 16-37). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Williams' central processor 101, coupled with bus 100 for processing information and instructions, of the ATPG system 12 to include Gittinger's a DMA (Direct Memory Access) control unit 20. The artisan would be motivated to do so because Williams does suggest that testing circuitry can be incorporated on the DUT 16 and it would reduce the throughput of data flowing from the ATPG system 12 to the DUT 16.

Claims 5, 15, 25 and 35:

Williams does not explicitly teach an exception handler to handling illegal conditions such as infinite loops, however, Williams does teach that program instructions can be stored in the RAM 102, ROM 103, or the storage device 104. (Page 6, ¶ 54). Gittinger teaches a "watchdog timer" (exception handler) is initialized by a software instruction just prior to performing an instruction or instructions which may result in an infinite hang condition (e.g. infinite loop, an instruction which never completes executing because data is never returned from an external device, etc.). (See col. 7, lines 31-44). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the software in Williams' ATPG system 12 to include Gittinger's "watchdog timer". The artisan would be motivated to do so because it would allow Williams to provide an interrupt that would cause the processor to exit from the instruction code that is experiencing the infinite hang condition.

Claims 7, 17, 27 and 36:

Williams teaches the ATPG tool 12 generates a set of test patterns that are used to locate faults within the DUT 16 (generate test sequences). Williams further discloses that the tester 14 applies the test patterns to the DUT 16 (runs the test sequences) and examines the real output of the DUT 16 against the expected output (comparing test results with an expected test result). The tester 16 then recalls the output from the DUT 16. The test vectors provide the necessary inputs in order to detect the presence of faults within the DUT 16 (check for manufacturing faults). (Page 4, ¶ 34). Williams does not explicitly teach that the microprocessor performs these steps. However, Williams

does suggest that testing circuitry, like the LFSR 230, can be incorporated on the DUT 16. (Page 5, ¶ 46). It would have been obvious to one of ordinary skill in the art at the time the invention was made to move the test sequence generation and execution functions to the DUT 16. Gittinger teaches a microcontroller 10 which a processor core 16, a DMA (Direct Memory Access) control unit 20 and an internal memory 30. Gittinger also teaches the DMA control unit 20 (software within the FRIT kernel is executed) is employed to initialize internal memory 30 to a selected background pattern and then to perform read and write tests of the background pattern and the complement of the background pattern upon internal memory 30. (Col. 8, lines 16-37). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Williams' central processor 101, coupled with bus 100 for processing information and instructions, of the ATPG system 12 to include Gittinger's a DMA (Direct Memory Access) control unit 20. It also would have been obvious to one of ordinary skill in the art at the time the invention was made to move the test sequence generation and execution functions to the DUT 16. The artisan would be motivated to do so because Williams does suggest that testing circuitry can be incorporated on the DUT 16 and it would reduce the throughput of data flowing from the ATPG system 12 to the DUT 16.

Claims 8, 18 and 28:

Williams teaches the ATPG tool 12 (FRIT kernel/SBE) contains a netlist description 18 of the electronic design that is found within the DUT 16 and can be written in HDL (high level design language) (computer model). Williams further teaches the ATPG tool 12 not only generates test patterns, but during simulation it also captures

the expected outputs of the netlist 18 (expected test result obtained from computer modeling) based on the application of these test patterns. (Page 3-4, ¶ 33).

Claims 9, 19, 29 and 37:

Williams does not explicitly teach generating a number of instruction sequences, however, Williams does teach that program instructions can be stored in the RAM 102, ROM 103, or the storage device 104. (Page 6, ¶ 54). Gittinger suggests instructions that may be performed by tester 42 for looping multiple passes of selected test patterns for microcontroller 10 depicted in FIG. 8. The code may be extended to perform passes for all selected patterns by storing the patterns in memory and using a counter to select the patterns and loop through the code a number of times equal to the number of selected patterns. (See col. 18, lines 11-17). It would have been obvious to one of ordinary skill in the art at the time the invention was made that Gittinger's looping instructions for testing a combination of multiple passes through number of selected test patterns can be programmed into Williams' program instructions in the RAM 102, ROM 103, or the storage device 104. The artisan would be motivated to do so because this would add flexibility to test multiple patterns successively and increase the testability of the microprocessor.

Claims 10, 20, 30 and 38:

Williams teaches the MISR generates a signature value (generates signatures). Williams also teaches the ATPG tool (SPE) can simulate the expected resultant signature, and this value is stored in memory 545. Therefore, circuit 540 can compare the expected final signature against the actual final signature as stored in signature

latch 535. If there are any errors or mismatches, the error flag 550 is set. If the error flag 550 is ever set, then verification for the DUT fails (test sequence is good or bad). (Page 7, ¶ 563).

***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John J. Tabone, Jr.
Examiner
Art Unit 2133

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